

REMARKS

Applicant respectfully requests reconsideration of the present U.S. patent application. Claims 1-5, 7-17 and 19-21 stand rejected under 35 U.S.C. § 103. Claims 1-4, 7, 9, 11, 13, 15, 17 and 20 have been amended. Claim 22 has been added. No claims have been canceled. Therefore, claims 1-5, 7-17 and 19-22 are pending.

Claim Rejections - 35 U.S.C. §103

Rejections of Claims 1 and 11-16 based on *Taniguchi*, *Holt* and *Apel*

Claims 1 and 11-16 were rejected under 35 U.S.C. §103 as being obvious over U.S. Patent No. 5,162,756 issued to Taniguchi et al. (*Taniguchi*), in view of Electronic Circuits – Digital and Analog by Holt (*Holt*) and U.S. Patent No. 6,894,561 issued to Apel (*Apel*). For at least the reasons set forth below, Applicant submits that claims 1 and 11-16 are not rendered obvious by *Taniguchi* in view of *Holt* and *Apel*.

Claim 1 recites the following:

a first transistor coupled to an input terminal, to receive a non-delayed input signal, and in response, provide an output signal;
a delay circuit configured to introduce a first delay to the non-delayed input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the non-delayed input signal received by the first transistor;
a second transistor coupled to the input terminal via the first delay circuit, to receive the delayed input signal, and in response, provide a first delayed output signal;...

Claim 15 recites similar limitations.

Taniguchi discloses a high-frequency signal power divider/combiner. See Fig. 2; col. 3, lines 7-16 and 55-56. The divider/combiner contains quarter wavelength transmission lines and field effect transistors (FETs). See Fig. 2; col. 3, lines 37-38 and 55-59. According to the Examiner, the combination of a first transmission line and a first FET receives an input signal, while a second transmission line receives the input signal, delays the input signal, because all the

quarter wavelength lines of *Taniguchi* delay signals, and provides the delayed input signal to a second FET. See Office Action, page 4, first paragraph.

Applicant does not agree with Examiners interpretations of *Taniguchi* and expressly reserves the right to refute such interpretations in any future office actions, if necessary. However, even under the Examiner's interpretation of *Taniguchi*, the first transistor receives a delayed signal, and the second FET receives a delayed signal. Consequently, *Taniguchi* does not disclose a first transistor coupled to an input terminal, to receive a non-delayed input signal, and in response, provide an output signal; a delay circuit configured to introduce a first delay to the non-delayed input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the non-delayed input signal received by the first transistor; and a second transistor coupled to the input terminal via the first delay circuit, to receive the delayed input signal, and in response, provide a first delayed output signal. Therefore, *Taniguchi* fails to disclose at least one limitation of claims 1 and 15.

Applicant agrees with Examiner that *Taniguchi* does not disclose the level control circuit and bias control circuitry of claims 1 and 15. See Office Action, page 4, first paragraph. Applicant does not necessarily agree with Examiner's other interpretations of *Taniguchi* and expressly reserves the right to refute such interpretations in any future office actions if necessary.

According to the Examiner, *Holt* teaches a bias circuit and level control circuit, and it would have been obvious to provide *Taniguchi* with such circuits. See Office Action pages 4-5. However, although a bias control circuit may be a necessary part of an amplifier circuit, *Holt* teaches no more than basic principles and theories of electronic circuits. *Holt* does not disclose the bias control circuitry or level control circuit of claims 1 and 15. In addition, Examiner does not contend that *Holt* discloses a first transistor coupled to an input terminal, to receive a non-delayed input signal, and in response, provide an output signal; a delay circuit configured to

introduce a first delay to the non-delayed input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the non-delayed input signal received by the first transistor; and a second transistor coupled to the input terminal via the first delay circuit, to receive the delayed input signal, and in response, provide a first delayed output signal, as recited in claims 1 and 15. Therefore, *Holt* fails to cure the deficiencies of *Taniguchi* pointed out by the Examiner or the deficiencies pointed out by the Applicant.

According to the Examiner, “*Holt* teaches that it is well known to provide a bias circuit ... so that [an] amplifier can operate ... so that non-linear operation is obtained.” See Office Action, pages 4-5. In addition, Examiner contends that it would have been obvious “to provide the combination of *Taniguchi* and *Holt* with a bias control circuitry such as that of *Apel*” See Office Action, page 6, paragraph 2.

Again, *Holt* teaches no more than basic principles and theories of electronic circuits, and does not disclose the bias control circuitry or level control circuit of claims 1 and 15. Applicant does not necessarily agree with Examiner’s interpretations of *Holt* or *Apel* and expressly reserves the right to refute such interpretations in any future office actions if necessary. However, it is clear that *Taniguchi*, *Holt* and *Apel* would not be combined to provide a bias control circuitry to enable transistors to operate in a saturated mode, as recited in claims 1 and 15, because *Apel* explicitly states that the advantage of the approach disclosed in *Apel* is in linearity, and that in all power states, high or low, RF transistors are biased for linear performance. See col. 3, lines 13-16. In addition, Examiner does not contend that *Apel* discloses a first transistor coupled to an input terminal, to receive a non-delayed input signal, and in response, provide an output signal; a delay circuit configured to introduce a first delay to the non-delayed input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the non-delayed input signal received by the first transistor; and a second transistor coupled to the input terminal

via the first delay circuit, to receive the delayed input signal, and in response, provide a first delayed output signal.

Therefore, *Apel* fails to cure the deficiencies of *Taniguchi* and *Holt* pointed out by the Examiner or the deficiencies pointed out by the Applicant. Thus, *Taniguchi* in view of *Holt* and *Apel* fails to disclose at least one limitation of claims 1 and 15. Consequently, claims 1 and 15 are not rendered obvious by *Taniguchi* in view of *Holt* and *Apel* for at least the reasons set forth above. Applicant therefore respectfully requests that the Examiner withdraw the rejections of claims 1 and 15 under 35 U.S.C. § 103.

Claims 11-14 and 22 depend from claim 1. Claim 16 depends from claim 15. Because dependent claims include the limitations of the claims from which they depend, Applicant submits that claims 11-14, 16 and 22 are not rendered obvious by *Taniguchi* in view of *Holt* and *Apel* for at least the reasons set forth above.

Rejections of Claims 2-4, 17 and 20 based on *Taniguchi*, *Holt*, *Apel* and *Cheng*

Claims 2-4, 17 and 20 were rejected under 35 U.S.C. § 103 as being unpatentable over *Taniguchi* in view of *Holt* and *Apel*, and further in view of Cheng et al., U.S. Patent Application No. 2002/0190790 (*Cheng*). For at least the reasons set forth below, Applicant submits that claims 2-4, 17 and 20 are not rendered obvious by *Taniguchi* in view of *Holt*, *Apel* and *Cheng*.

Cheng was cited as teaching selectively supplying bias voltages to each of parallel-connected amplifiers. See Office Action page 7. As explained above, *Taniguchi* in view of *Holt* and *Apel* fails to disclose a first transistor coupled to an input terminal, to receive a non-delayed input signal, and in response, provide an output signal; a delay circuit configured to introduce a first delay to the non-delayed input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the non-delayed input signal received by the first

transistor; and a second transistor coupled to the input terminal via the first delay circuit, to receive the delayed input signal, and in response, provide a first delayed output signal, as recited in claims 1 and 15. Examiner does not assert that *Cheng* discloses these limitations of claims 1 and 15.

Applicant does not necessarily agree with Examiner's interpretation of *Cheng* and expressly reserves the right to refute such interpretations in any future office actions if necessary. However, regardless of whether Examiner's interpretations of *Cheng* are correct, *Cheng* fails to cure the deficiencies of *Taniguchi* in view of *Holt* and *Apel* explained above. Thus, *Taniguchi* in view of *Holt*, *Apel* and *Cheng* fails to disclose at least one limitation of claims 1 and 15. Consequently, claims 1 and 15 are not rendered obvious by *Taniguchi* in view of *Holt*, *Apel* and *Cheng* for at least the reasons set forth above.

Claims 2-4 depend from claim 1. Claims 17 and 20 depend from claim 15. Because dependent claims include the limitations of the claims from which they depend, Applicant submits that claims 2-4, 17 and 20 are not rendered obvious by *Taniguchi* in view of *Holt*, *Apel* and *Cheng* for at least the reasons set forth above with regard to claims 1 and 15. Applicant therefore respectfully requests that the Examiner withdraw the rejections of claims 2-4, 17 and 20 under 35 U.S.C. § 103.

Rejection of Claim 21 based on *Taniguchi*, *Holt*, *Cheng*, *Apel* and *Atwater*

Claim 21 was rejected under 35 U.S.C. § 103 as being unpatentable over *Taniguchi* in view of *Holt*, *Apel* and *Cheng*, and further in view of U.S. Patent No. 4,189,732 issued to *Atwater* (*Atwater*). For at least the reasons set forth below, Applicant submits that claim 21 is not rendered obvious by *Taniguchi* in view of *Holt*, *Apel*, *Cheng* and *Atwater*.

Atwater was cited as teaching a circuit for providing a power supply voltage to an amplifier. See Office Action page 7. As explained above, *Taniguchi* in view of *Holt*, *Apel* and *Cheng* fails to disclose providing an input signal to a first transistor in a low power mode, wherein the input signal is non-delayed; introducing a first delay to the non-delayed input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the input signal received by the first transistor; and providing the delayed input signal to a second transistor, as recited in claim 15. Examiner does not assert that *Atwater* discloses these limitations of claim 15.

Applicant does not necessarily agree with Examiner's interpretation of *Atwater* and expressly reserves the right to refute such interpretations in any future office actions if necessary. However, regardless of whether Examiner's interpretations of *Atwater* are correct, *Atwater* fails to cure the deficiencies of *Taniguchi* in view of *Holt*, *Apel* and *Cheng* explained above. Thus, *Taniguchi* in view of *Holt*, *Apel*, *Cheng* and *Atwater* fails to disclose at least one limitation of claim 15. Consequently, claim 15 is not rendered obvious by *Taniguchi* in view of *Holt*, *Apel*, *Cheng* and *Atwater* for at least the reasons set forth above.

Claim 21 depends from claim 15. Because dependent claims include the limitations of the claims from which they depend, Applicant submits that claim 21 is not rendered obvious by *Taniguchi* in view of *Holt*, *Apel*, *Cheng* and *Atwater* for at least the reasons set forth above with regard to claim 15. Applicant therefore respectfully requests that the Examiner withdraw the rejections of claim 21 under 35 U.S.C. § 103.

Rejections of Claims 5, 7-10 and 19 based on *Taniguchi*, *Holt*, *Apel* and *Atwater*

Claims 5, 7-10 and 19 were rejected under 35 U.S.C. § 103 as being unpatentable over *Taniguchi* in view of *Holt* and *Apel*, and further in view of *Atwater*. For at least the reasons set

forth below, Applicant submits that claims 5, 7-10 and 19 are not rendered obvious by *Taniguchi* in view of *Holt*, *Apel* and *Atwater*.

Atwater was cited with regard to a power supply circuit. See Office Action, page 8. As explained above, *Taniguchi* in view of *Holt* and *Apel* fails to disclose a first transistor coupled to an input terminal, to receive a non-delayed input signal, and in response, provide an output signal; a delay circuit configured to introduce a first delay to the non-delayed input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the non-delayed input signal received by the first transistor; and a second transistor coupled to the input terminal via the first delay circuit, to receive the delayed input signal, and in response, provide a first delayed output signal, as recited in claims 1 and 15. Examiner does not assert that *Atwater* discloses these limitations of claims 1 and 15.

Again, Applicant does not necessarily agree with Examiner's interpretation of *Atwater* and expressly reserves the right to refute such interpretations in any future office actions if necessary. However, regardless of whether Examiner's interpretations of *Atwater* are correct, *Atwater* fails to cure the deficiencies of *Taniguchi* in view of *Holt* and *Apel* explained above. Thus, *Taniguchi* in view of *Holt*, *Apel* and *Atwater* fails to disclose at least one limitation of claims 1 and 15. Consequently, claims 1 and 15 are not rendered obvious by *Taniguchi* in view of *Holt*, *Apel* and *Atwater* for at least the reasons set forth above.

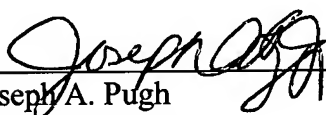
Claims 5 and 7-10 depend from claim 1. Claim 19 depends from claim 15. Because dependent claims include the limitations of the claims from which they depend, Applicant submits that claims 5, 7-10 and 19 are not rendered obvious by *Taniguchi* in view of *Holt*, *Apel* and *Atwater* for at least the reasons set forth above with regard to claims 1 and 15. Applicant therefore respectfully requests that the Examiner withdraw the rejections of claims 5, 7-10 and 19 under 35 U.S.C. § 103.

CONCLUSION

For at least the foregoing reasons, Applicant submits that the rejections have been overcome. Therefore, claims 1-5, 7-17 and 19-22 are in condition for allowance and such action is respectfully solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the application.

Respectfully submitted,

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